Table XIV. Standby Mode Operation

I/O Block	Standby 3 (Default)[1,2]	OUT_CONT = LO[2,3]	Standby 2[3,4]	Standby 1[3,4]
AFE	OFF	No Change	OFF	Only REFT, REFB ON
Timing Core	OFF	No Change	OFF	ON
CLO Oscillator	OFF	No Change	ON	ON
CLO	HI	Running	Running	Running
V1	LO	LO	LO	LO
V2	LO	LO	LO	LO
V3	LO	LO	LO	LO
V4	LO	LO	LO	LO
V5	LO	HI	HI	HI
V6	LO	HI	HI	HI
VSG1	LO	HI	HI	HI
VSG2	LO	HI	HI	HI
VSG3	LO	HI	HI	HI
VSG4	LO	HI	HI	HI
VSG5	LO	HI	HI	HI
SUBCK	LO	HI	HI	HI
VSUB	LO	LO	LO	LO
MSHUT	LO	LO	LO	LO
STROBE	LO	LO	LO	LO
H1	Hi-Z	LO	LO (4.3 mA)	LO (4.3 mA)
H2	Hi-Z	HI	HI (4.3 mA)	HI (4.3 mA)
H3	Hi-Z	LO	LO (4.3 mA)	LO (4.3 mA)
H4	Hi-Z	HI	HI (4.3 mA)	HI (4.3 mA)
RG	Hi-Z	LO	LO (4.3 mA)	LO (4.3 mA)
VD	LO	VDHDPOL Value	VDHDPOL Value	Running
HD	LO	VDHDPOL Value	VDHDPOL Value	Running
DCLK	LO	LO	LO	Running
DOUT	LO	LO	LO	LO

NOTES
[1] To exit Standby 3, first write 00 to OPRMODE[1:0], then reset the Timing Core after ~500 µs to guarantee proper settling of the oscillator.
[2] Standby 3 mode takes priority over OUT_CONTROL for determining the output polarities.
[3] These polarities assume OUT_CONT = HI because OUT_CONTROL = LO takes priority over Standby 1 and 2.
[4] Standby 1 and 2 will set H and RG drive strength to minimum value (4.3 mA).

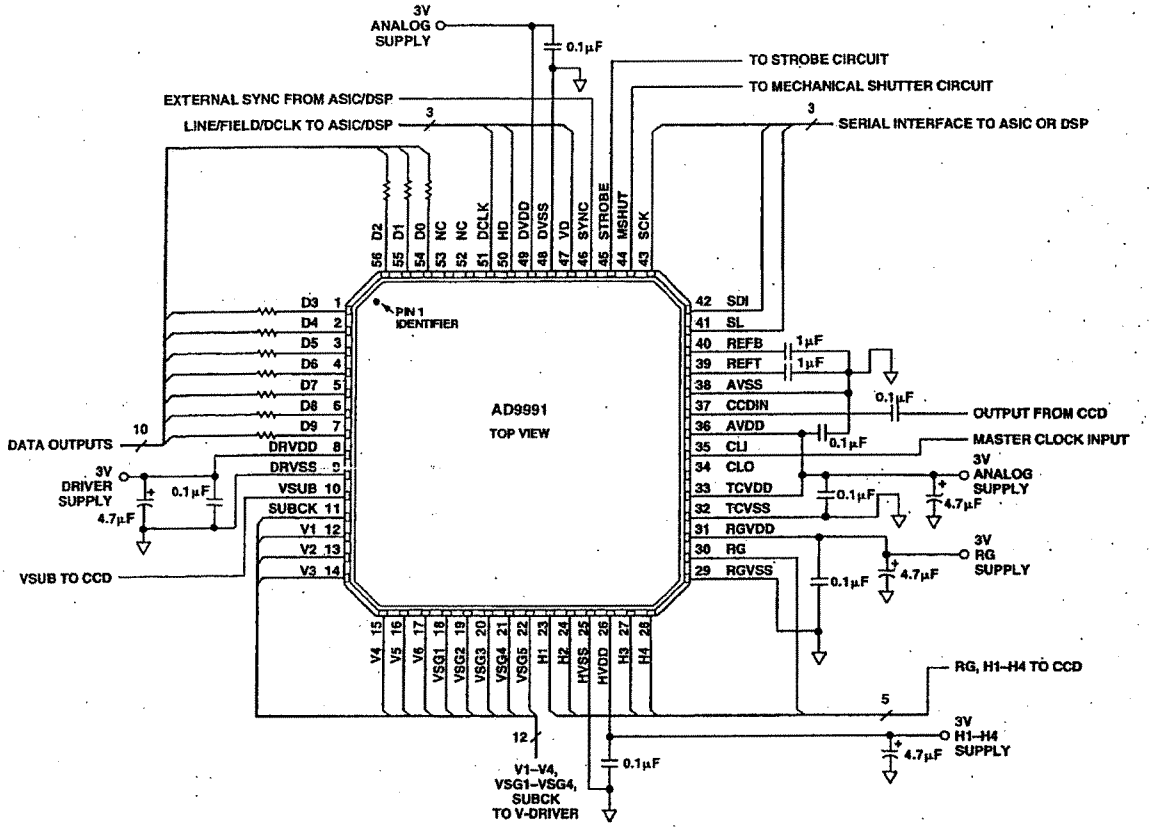


Figure 38. AD9991 Typical Circuit Configuration

CIRCUIT LAYOUT INFORMATION

The AD9991 typical circuit connection is shown in Figure 38. The PCB layout is critical in achieving good image quality from the AD999x products. All of the supply pins, particularly the AVDD1, TCVDD, RGVDD, and HVDD supplies, must be decoupled to ground with good quality high frequency chip capacitors. The decoupling capacitors should be located as close as possible to the supply pins, and should have a very low impedance path to a continuous ground plane. There should also be a 4.7 µF or larger value bypass capacitor for each main supply—AVDD, RGVDD, HVDD, and DRVDD—although this is not necessary for each individual pin. In most applications, it is easier to share the supply for RGVDD and HVDD, which may be done as long as the individual supply pins are separately bypassed. A separate 3 V supply may also be used for DRVDD, but this supply pin should still be decoupled to the same ground plane as the rest of the chip. A separate ground for DRVSS is not recommended. It is recommended that the exposed paddle on the bottom of the package be soldered to a large pad, with multiple vias connecting the pad to the ground plane.

The analog bypass pins (REFT, REFB) should also be carefully decoupled to ground as close as possible to their respective pins. The analog input (CCDIN) capacitor should also be located close to the pin.

The H1–4 and RG traces should be designed to have low inductance to avoid excessive distortion of the signals. Heavier traces are recommended because of the large transient current demand on H1–4 by the CCD. If possible, physically locating the AD9991 closer to the CCD will reduce the inductance on these lines. As always, the routing path should be as direct as possible from the AD9991 to the CCD.

The AD9991 also contains an on-chip oscillator for driving an external crystal. Figure 39 shows an example application using a typical 24 MHz crystal. For the exact values of the external resistors and capacitors, it is best to consult with the crystal manufacturer's data sheet.

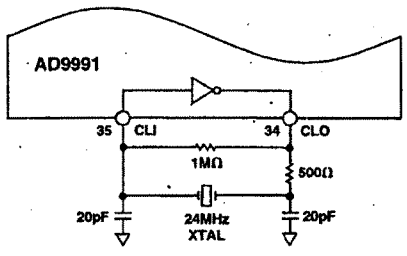
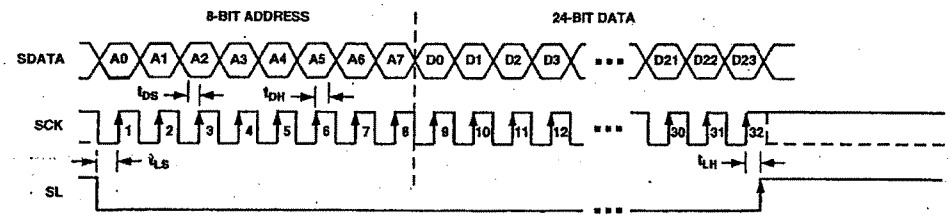


Figure 39. Crystal Driver Application

SERIAL INTERFACE TIMING

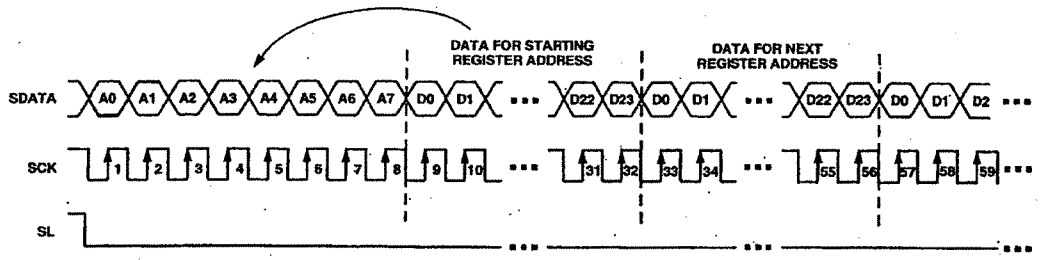
All of the internal registers of the AD9991 are accessed through a 3-wire serial interface. Each register consists of an 8-bit address and a 24-bit data-word. Both the 8-bit address and 24-bit data-word are written starting with the LSB. To write to each register, a 32-bit operation is required, as shown in Figure 40a. Although many registers are fewer than 24 bits wide, all 24 bits must be written for each register. For example, if the register is only 10 bits wide, the upper 14 bits are don't cares and may be filled with 0s during the serial write operation. If fewer than 24 bits are written, the register will not be updated with new data.

Figure 40b shows a more efficient way to write to the registers, using the AD9991's address auto-increment capability. Using this method, the lowest desired address is written first, followed by multiple 24-bit data-words. Each new 24-bit data-word will automatically be written to the next highest register address. By eliminating the need to write each 8-bit address, faster register loading is achieved. Continuous write operations may be used starting with any register location, and may be used to write to as few as two registers, or as many as the entire register space.



NOTES
1. SDATA BITS ARE LATCHED ON SCK RISING EDGES. SCK MAY IDLE HIGH OR LOW IN BETWEEN WRITE OPERATIONS.
2. ALL 32 BITS MUST BE WRITTEN: 8 BITS FOR ADDRESS AND 24 BITS FOR DATA.
3. IF THE REGISTER LENGTH IS <24 BITS, "DON'T CARE" BITS MUST BE USED TO COMPLETE THE 24-BIT DATA LENGTH.
4. NEW DATA VALUES ARE UPDATED IN THE SPECIFIED REGISTER LOCATION AT DIFFERENT TIMES, DEPENDING ON THE PARTICULAR REGISTER WRITTEN TO. SEE THE REGISTER UPDATES SECTION FOR MORE INFORMATION.

Figure 40a. Serial Write Operation



NOTES
1. MULTIPLE SEQUENTIAL REGISTERS MAY BE LOADED CONTINUOUSLY.
2. THE FIRST (LOWEST ADDRESS) REGISTER ADDRESS IS WRITTEN, FOLLOWED BY MULTIPLE 24-BIT DATA-WORDS.
3. THE ADDRESS WILL AUTOMATICALLY INCREMENT WITH EACH 24-BIT DATA-WORD (ALL 24 BITS MUST BE WRITTEN).
4. SL IS HELD LOW UNTIL THE LAST DESIRED REGISTER HAS BEEN LOADED.

Figure 40b. Continuous Serial Write Operation

Register Address Banks 1 and 2

The AD9991 address space is divided into two different register banks, referred to as Register Bank 1 and Register Bank 2. Figure 41 illustrates how the two banks are divided. Register Bank 1 contains the registers for the AFE, miscellaneous functions, VD/HD parameters, timing core, CLPOB masking, VSG patterns, and shutter functions. Register Bank 2 contains all of the information for the V-pattern groups, V-sequences, and field information.

When writing to the AD9991, address 0x7F is used to specify which address bank is being written to. To write to Bank 1, the LSB of address 0x7F should be set to 0; to write to Bank 2, the LSB of address 0x7F should be set to 1.

Note that Register Bank 1 contains many unused addresses. Any undefined addresses between address 0x00 and 0x7F are considered don't cares, and it is acceptable if these addresses are filled in with all 0s during a continuous register write operation. However, the undefined addresses above 0x7F must not be written to, or the AD9991 may not operate properly.

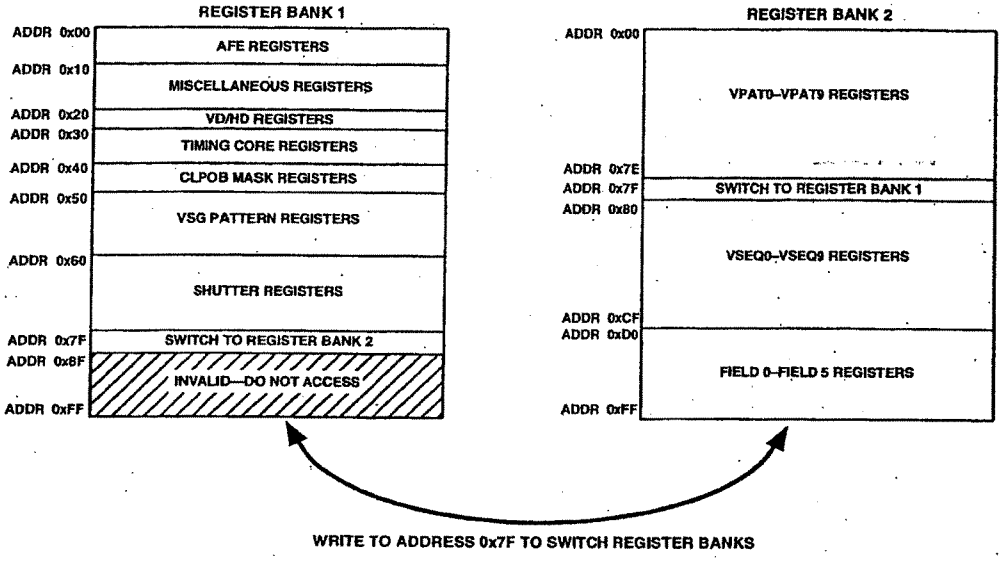


Figure 41. Layout of Internal Register Banks 1 and 2

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Updating of New Register Values

The AD9991's internal registers are updated at different times, depending on the particular register. Table XV summarizes the four different types of register updates:

1. **SCK Updated:** Some of the registers in Bank 1 are updated immediately, as soon as the 24th data bit (D23) is written. These registers are used for functions that do not require gating with the next VD boundry, such as power-up and reset functions. These registers are lightly shaded in gray in the Bank 1 register list.

   The Bank Select register (addr 0x7F in Bank 1 and 2) is also SCK updated.

2. **VD Updated:** Most of the registers in Bank 1, as well as the Field registers in Bank 2, are updated at the next VD falling edge. By updating these values at the next VD edge, the current field will not be corrupted and the new register values will be applied to the next field. The Bank 1 register updates may be further delayed past the VD falling edge by using the UPDATE register (addr 0x19). This will delay the VD updated register updates to any HD line in the field. Note that the Bank 2 registers are not affected by the UPDATE register.

3. **SG-Line Updated:** A few of the registers in Bank 1 are updated at the end of the SG active line, at the HD falling edge. These are the registers to control the SUBCK signal so that the SUBCK output will not be updated until after the SG line has been completed. These registers are darkly shaded in gray in the Bank 1 register list.

4. **SCP Updated:** In Bank 2, all of the V-pattern group and V-sequence registers (addr 0x00 through 0xCF, excluding 0x7F) are updated at the next SCP, where they will be used. For example, in Figure 42, this field has selected Region 1 to use V-Sequence 3 for the vertical outputs. This means that a write to any of the V-Sequence 3 registers, or any of the V-pattern group registers that are referenced by V-Sequence 3 will be updated at SCP1. If multiple writes are done to the same register, the last one done before SCP1 will be the one that is updated. Likewise, register writes to any V-Sequence 5 registers will be updated at SCP2, and register writes to any V-Sequence 8 registers will be updated at SCP3.

Table XV. Register Update Locations

Update Type	Register Bank	Description
SCK Updated	Bank 1 Only	Register is immediately updated when the 24th data bit (D23) is clocked in.
VD Updated	Bank 1 and Bank 2	Register is updated at the VD falling edge. VD updated registers in Bank 1 may be delayed further by using the UPDATE register at address 0x19 in Bank 1. Bank 2 updates will not be affected by the UPDATE register.
SG Line Updated	Bank 1 Only	Register is updated at the HD falling edge at the end of the SG-active line.
SCP Updated	Bank 2 Only	Register is updated at the next SCP when the register will be used.

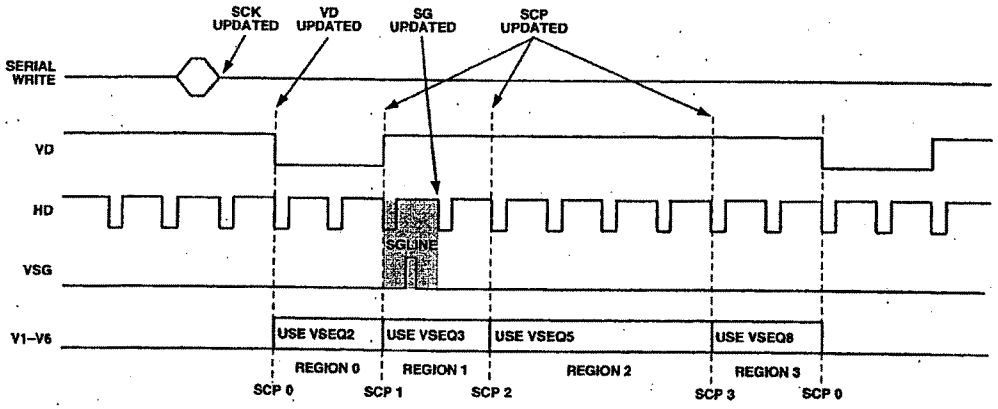

Figure 42. Register Update Locations (See Table XV for Definitions)

COMPLETE LISTING FOR REGISTER BANK 1
All registers are VD updated, except where noted: = SCK Updated = SG-Line Updated
All address and default values are in hexadecimal.

Table XVI. AFE Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
00	[11:0]	7	OPRMODE	AFE Operation Modes (See Table XXIV for Detail)
01	[9:0]	0	VGAGAIN	VGA Gain.
02	[7:0]	80	CLAMPLEVEL	Optical Black Clamp Level.
03	[11:0]	4	CTLMODE	AFE Control Modes (See Table XXV for Detail)

Table XVII. Miscellaneous Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
10	[0]	0	SW_RST	Software Reset. 1 = Reset all registers to default, then self-clear back to 0.
11	[0]	0	OUTCONTROL	Output Control. 0 = Make all outputs dc inactive.
12	[0]	1	TEST_USE	Internal Use Only. Must be set to 1.
13	[0]	0	SYNCPOL	SYNC Active Polarity (0 = Active Low).
14	[0]	0	SYNCSUSPEND	Suspend Clocks during SYNC Active (1 = Suspend).
15	[0]	0	TGCORE_RSTB	Timing Core Reset Bar. 0 = Reset TG Core, 1 = Resume Operation.
16	[0]	1	OSC_PWRDOWN	CLO Oscillator Power-Down (0 = Oscillator is powered down).
17				Unused.
18	[0]	0	TEST_USE	Internal Use Only. Must be set to 0.
19	[11:0]	0	UPDATE	Serial Update. Line (HD) in the field to update VD updated registers.
1A	[0]	0	PREVENTUPDATE	Prevents the Update of the VD Updated Registers. 1 = Prevent update.
1B	[23:0]	0	MODE	Mode Register.
1C	[1:0]	0	FIELDVAL	Field Value Sync. 0 = Next Field 0, 1 = Next Field 1, 2/3 = Next Field 2.

Table XVIII. VD/HD Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
20	[0]	0	MASTER	VD/HD Master or Slave Timing (0 = Slave Mode)
21	[0]	0	VDHDPOL	VD/HD Active Polarity 0 = Low, 1 = High
22	[17:0]	0	VDHDRISE	Rising Edge Location for VD [17:12] and HD [11:0].

Table XIX. Timing Core Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
30	[0]	0	CLIDIVIDE	Divide CLI Input Clock by 2. 1 = Divide by 2.
31	[12:0]	01001	H1CONTROL	H1 Signal Control. Polarity [0] (0 = Inversion, 1 = No Inversion). H1 Positive Edge Location [6:1]. H1 Negative Edge Location [12:7].
32	[12:0]	01001	H2CONTROL	H2 Signal Control. Polarity [0] (0 = Inversion, 1 = No Inversion). H2 Positive Edge Location [6:1]. H2 Negative Edge Location [12:7].
33	[12:0]	00801	RGCONTROL	RG Signal Control. Polarity [0] (0 = Inversion, 1 = No Inversion). RG Positive Edge Location [6:1]. RG Negative Edge Location [12:7].
34	[1:0]	0	HBLKRETIME	Retime HBLK to Internal H1/H2 Clocks. H1 Retime [0]. H2 Retime [1]. Preferred setting is 1 for each bit. Setting each bit to 1 will add one cycle delay to HBLK toggle positions.
35	[14:0]	1249	DRVCONTROL	Drive Strength Control for H1 [2:0], H2 [5:3], H3 [8:6], H4 [11:9], and RG [14:12]. Drive Current Values: 0 = Off, 1 = 4.3 mA, 2 = 8.6 mA, 3 = 12.9 mA, 4 = 17.2 mA, 5 = 21.5 mA, 6 = 25.8 mA, 7 = 30.1 mA.
36	[11:0]	00024	SAMPCONTROL	SHP/SHD Sample Control. SHP Sampling Location [5:0]. SHD Sampling Location [11:6].
37	[8:0]	100	DOUTCONTROL	DOUT Phase Control [5:0]. DCLK Mode [6]. DOUTDELAY [8:7].

Table XX. CLPOB Masking Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
40	[23:0]	FFFFFF	CLPMASK01	CLPOB Line Masking. Line #0 [11:0]. Line #1 [23:0].
41	[23:0]	FFFFFF	CLPMASK23	CLPOB Line Masking. Line #2 [11:0]. Line #3 [23:0].
42	[11:0]	FFFFFF	CLPMASK4	CLPOB Line Masking. Line #4 [11:0].

Table XXI. SG Pattern Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
50	[3:0]	F	SGPOL	Start Polarity for SG Patterns. Pattern #0 [0]. Pattern #1 [1]. Pattern #2 [2]. Pattern #3 [3].
51	[23:0]	FFFFFF	SGTOG12_0	Pattern #0. Toggle Position 1 [11:0]. Toggle Position 2 [23:12].
52	[23:0]	FFFFFF	SGTOG12_1	Pattern #1. Toggle Position 1 [11:0]. Toggle Position 2 [23:12].
53	[23:0]	FFFFFF	SGTOG12_2	Pattern #2. Toggle Position 1 [11:0]. Toggle Position 2 [23:12].
54	[23:0]	FFFFFF	SGTOG12_3	Pattern #3. Toggle Position 1 [11:0]. Toggle Position 2 [23:12].

Table XXII. Shutter Control Register Map

Address	Data Bit Content	Default Value	Register Name	Register Description
60	[4:0]	0	TRIGGER	Trigger for VSUB [0], MSHUT [1], STROBE [2], Exposure [3], and Readout [4]. Note that to trigger the Readout to automatically occur after the Exposure period, both Exposure and Readout should be triggered together.
61	[2:0]	2	READOUT	Number of Fields to Suppress the SUBCK Pulses after the VSG Line.
62	[11:0] [12]	0 0	EXPOSURE VDHDOFF	Number of Fields to Suppress the SUBCK and VSG Pulses. Set = 1 to Disable the VD/HD Outputs during exposure (when >1 field).
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

Table XXII. Shutter Control Register Map (continued)

Address	Data Bit Content	Default Value	Register Name	Register Description
67	[1:0]	0	VSUBMODE	VSUB Readout Mode [0]. VSUB Keep-On Mode [1].
68	[12:0]	1000	VSUBON	VSUB ON Position [11:0]. VSUB Active Polarity [12].
69	[1:0]	1	MSHUTPOL	MSHUT Active Polarity [0]. MSHUT Manual Enable [1].
6A	[23:0]	0	MSHUTON	MSHUT ON Position. Line [11:0]. Pixel [23:0].
6B	[11:0]	0	MSHUTOFF_FD	MSHUT OFF Field Position.
6C	[23:0]	0	MSHUTOFF_LNPX	MSHUT OFF Position. Line [11:0]. Pixel [23:12].
6D	[0]	1	STROBPOL	STROBE Active Polarity.
6E	[11:0]	0	STROBON_FD	STROBE ON Field Position.
6F	[23:0]	0	STROBON_LNPX	STROBE ON Position. Line [11:0]. Pixel [23:12].
70	[11:0]	0	STROBOFF_FD	STROBE OFF Field Position.
71	[23:0]	0	STROBOFF_LNPX	STROBE OFF Position. Line [11:0]. Pixel [23:12].

Table XXIII. Register Map Selection

Address	Data Bit Content	Default Value	Register Name	Register Description
7F	[0]	0	BANKSELECT1	Register Bank Access from Bank 1 to Bank 2. 0 = Bank 1, 1 = Bank 2.

Table XXIV. AFE Operation Register Detail

Address	Data Bit Content	Default Value	Register Name	Register Description
00	[1:0]	3	PWRDOWN	0 = Normal Operation, 1 = Standby 1, 2 = Standby 2, 3 = Standby 3.
	[2]	1	CLPENABLE	0 = Disable OB Clamp, 1 = Enable OB Clamp.
	[3]	0	CLPSPEED	0 = Select Normal OB Clamp Settling, 1 = Select Fast OB Clamp Settling.
	[4]	0	TEST	Test Use Only. Set to 0.
	[5]	0	PBLK_LVL	DOUT Value during PBLK: 0 = Blank to Zero, 1 = Blank to Clamp Level.
	[7:6]	0	TEST	Test Use Only. Set to 0.
	[8]	0	DCBYP	0 = Enable DC Restore Circuit, 1 = Bypass DC Restore Circuit during PBLK.
	[9]	0	TEST	Test Use Only. Set to 0.

Table XXV. AFE Control Register Detail

Address	Data Bit Content	Default Value	Register Name	Register Description
03	[1:0]	0	TEST	Test Use Only. Set to 00.
	[2]	1	TEST	Test Use Only. Set to 1.
	[3]	0	DOUTDISABLE	0 = Data Outputs are Driven, 1 = Data Outputs are Three-Stated.
	[4]	0	DOUTLATCH	0 = Latch Data Outputs with DOUT Phase, 1 = Output Latch Transparent.
	[5]	0	GRAYENCODE	0 = Binary Encode Data Outputs, 1 = Gray Encode Data Outputs.

COMPLETE LISTING FOR REGISTER BANK 2
All V-pattern group and V-sequence registers are SCP updated, and all Field registers are VD updated.
All address and default values are in hexadecimal.

Table XXVI. V-Pattern Group 0 (VPAT0) Register Map

Address	Data Bit Content	Default Value	Register Name	Description
00	[5:0]	0	VPOL_0	VPAT0 Start Polarity. V1[0]. V2[1]. V3[2]. V4[3]. V5[4]. V6[5].
	[11:6]	0	UNUSED	Unused.
	[23:12]	0	VPATLEN_0	Total Length of VPAT0. Note: If using VPAT0 as a second V-sequence in the VSG active line, this value is the start position for second V-sequence.
01	[11:0]	0	V1TOG1_0	V1 Toggle Position 1
	[23:12]	0	V1TOG2_0	V1 Toggle Position 2
02	[11:0]	0	V1TOG3_0	V1 Toggle Position 3
	[23:12]	0	V2TOG1_0	V2 Toggle Position 1
03	[11:0]	0	V2TOG2_0	V2 Toggle Position 2
	[23:12]	0	V2TOG3_0	V2 Toggle Position 3
04	[11:0]	0	V3TOG1_0	V3 Toggle Position 1
	[23:12]	0	V3TOG2_0	V3 Toggle Position 2
05	[11:0]	0	V3TOG3_0	V3Toggle Position 3
	[23:12]	0	V4TOG1_0	V4 Toggle Position 1
06	[11:0]	0	V4TOG2_0	V4 Toggle Position 2
	[23:12]	0	V4TOG3_0	V4 Toggle Position 3
07	[11:0]	0	V5TOG1_0	V5 Toggle Position 1
	[23:12]	0	V5TOG2_0	V5 Toggle Position 2
08	[11:0]	0	V5TOG3_0	V5 Toggle Position 3
	[23:12]	0	V6TOG1_0	V6 Toggle Position 1
09	[11:0]	0	V6TOG2_0	V6 Toggle Position 2
	[23:12]	0	V6TOG3_0	V6 Toggle Position 3
0A	[11:0]	0	FREEZE1_0	V1–V6 Freeze Position 1
	[23:12]	0	RESUME1_0	V1–V6 Resume Position 1
0B	[11:0]	0	FREEZE2_0	V1–V6 Freeze Position 2
	[23:12]	0	RESUME2_0	V1–V6 Resume Position 2

Table XXVII. V-Pattern Group 1 (VPAT1) Register Map

Address	Data Bit Content	Default Value	Register Name	Description
0C	[5:0]	0	VPOL_1	VPAT1 Start Polarity. V1[0]. V2[1]. V3[2]. V4[3]. V5[4]. V6[5].
	[11:6]	0	UNUSED	Unused.
	[23:12]	0	VPATLEN_1	Total Length of VPAT1. Note: If using VPAT1 as a second V-sequence in the VSG active line, this value is the start position for second V-sequence.
0D	[11:0]	0	V1TOG1_1	V1 Toggle Position 1
	[23:12]	0	V1TOG2_1	V1 Toggle Position 2
0E	[11:0]	0	V1TOG3_1	V1 Toggle Position 3
	[23:12]	0	V2TOG1_1	V2 Toggle Position 1
0F	[11:0]	0	V2TOG2_1	V2 Toggle Position 2
	[23:12]	0	V2TOG3_1	V2 Toggle Position 3
10	[11:0]	0	V3TOG1_1	V3 Toggle Position 1
	[23:12]	0	V3TOG2_1	V3 Toggle Position 2
11	[11:0]	0	V3TOG3_1	V3Toggle Position 3
	[23:12]	0	V4TOG1_1	V4 Toggle Position 1
12	[11:0]	0	V4TOG2_1	V4 Toggle Position 2
	[23:12]	0	V4TOG3_1	V4 Toggle Position 3

Table XXVII. V-Pattern Group 1 (VPAT1) Register Map (continued)

Address	Data Bit Content	Default Value	Register Name	Description
13	[11:0] [23:12]	0 0	V5TOG1_1 V5TOG2_1	V5 Toggle Position 1 V5 Toggle Position 2
14	[11:0] [23:12]	0 0	V5TOG3_1 V6TOG1_1	V5 Toggle Position 3 V6 Toggle Position 1
15	[11:0] [23:12]	0 0	V6TOG2_1 V6TOG3_1	V6 Toggle Position 2 V6 Toggle Position 3
16	[11:0] [23:12]	0 0	FREEZE1_1 RESUME1_1	V1–V6 Freeze Position 1 V1–V6 Resume Position 1
17	[11:0] [23:12]	0 0	FREEZE2_1 RESUME2_1	V1–V6 Freeze Position 2 V1–V6 Resume Position 2

Table XXVIII. V-Pattern Group 2 (VPAT2) Register Map

Address	Data Bit Content	Default Value	Register Name	Description
18	[5:0] [11:6] [23:12]	0 0 0	VPOL_2 UNUSED VPATLEN_2	VPAT2 Start Polarity. V1[0]. V2[1]. V3[2]. V4[3]. V5[4]. V6[5]. Unused. Total Length of VPAT2. Note: If using VPAT2 as a second V-sequence in the VSG active line, this value is the start position for second V-sequence.
19	[11:0] [23:12]	0 0	V1TOG1_2 V1TOG2_2	V1 Toggle Position 1 V1 Toggle Position 2
1A	[11:0] [23:12]	0 0	V1TOG3_2 V2TOG1_2	V1 Toggle Position 3 V2 Toggle Position 1
1B	[11:0] [23:12]	0 0	V2TOG2_2 V2TOG3_2	V2 Toggle Position 2 V2 Toggle Position 3
1C	[11:0] [23:12]	0 0	V3TOG1_2 V3TOG2_2	V3 Toggle Position 1 V3 Toggle Position 2
1D	[11:0] [23:12]	0 0	V3TOG3_2 V4TOG1_2	V3 Toggle Position 3 V4 Toggle Position 1
1E	[11:0] [23:12]	0 0	V4TOG2_2 V4TOG3_2	V4 Toggle Position 2 V4 Toggle Position 3
1F	[11:0] [23:12]	0 0	V5TOG1_2 V5TOG2_2	V5 Toggle Position 1 V5 Toggle Position 2
20	[11:0] [23:12]	0 0	V5TOG3_2 V6TOG1_2	V5 Toggle Position 3 V6 Toggle Position 1
21	[11:0] [23:12]	0 0	V6TOG2_2 V6TOG3_2	V6 Toggle Position 2 V6 Toggle Position 3
22	[11:0] [23:12]	0 0	FREEZE1_2 RESUME1_2	V1–V6 Freeze Position 1 V1–V6 Resume Position 1
23	[11:0] [23:12]	0 0	FREEZE2_2 RESUME2_2	V1–V6 Freeze Position 2 V1–V6 Resume Position 2

Table XXIX. V-Pattern Group 3 (VPAT3) Register Map

Address	Data Bit Content	Default Value	Register Name	Description
24	[5:0] [11:6] [23:12]	0 0 0	VPOL_3 UNUSED VPATLEN_3	VPAT3 Start Polarity. V1[0]. V2[1]. V3[2]. V4[3]. V5[4]. V6[5]. Unused. Total Length of VPAT3. Note: If using VPAT3 as a second V-sequence in the VSG active line, this value is the start position for second V-sequence.
25	[11:0] [23:12]	0 0	V1TOG1_3 V1TOG2_3	V1 Toggle Position 1 V1 Toggle Position 2

Table XXIX. V-Pattern Group 3 (VPAT3) Register Map (continued)

Address	Data Bit Content	Default Value	Register Name	Description
26	[11:0]	0	V1TOG3_3	V1 Toggle Position 3
	[23:12]	0	V2TOG1_3	V2 Toggle Position 1
27	[11:0]	0	V2TOG2_3	V2 Toggle Position 2
	[23:12]	0	V2TOG3_3	V2 Toggle Position 3
28	[11:0]	0	V3TOG1_3	V3 Toggle Position 1
	[23:12]	0	V3TOG2_3	V3 Toggle Position 2
29	[11:0]	0	V3TOG3_3	V3 Toggle Position 3
	[23:12]	0	V4TOG1_3	V4 Toggle Position 1
2A	[11:0]	0	V4TOG2_3	V4 Toggle Position 2
	[23:12]	0	V4TOG3_3	V4 Toggle Position 3
2B	[11:0]	0	V5TOG1_3	V5 Toggle Position 1
	[23:12]	0	V5TOG2_3	V5 Toggle Position 2
2C	[11:0]	0	V5TOG3_3	V5 Toggle Position 3
	[23:12]	0	V6TOG1_3	V6 Toggle Position 1
2D	[11:0]	0	V6TOG2_3	V6 Toggle Position 2
	[23:12]	0	V6TOG3_3	V6 Toggle Position 3
2E	[11:0]	0	FREEZE1_3	V1–V6 Freeze Position 1
	[23:12]	0	RESUME1_3	V1–V6 Resume Position 1
2F	[11:0]	0	FREEZE2_3	V1–V6 Freeze Position 2
	[23:12]	0	RESUME2_3	V1–V6 Resume Position 2

Table XXX. V-Pattern Group 4 (VPAT4) Register Map

Address	Data Bit Content	Default Value	Register Name	Description
30	[5:0]	0	VPOL_4	VPAT4 Start Polarity. V1[0]. V2[1]. V3[2]. V4[3]. V5[4]. V6[5].
	[11:6]	0	UNUSED	Unused.
	[23:12]	0	VPATLEN_4	Total Length of VPAT4. Note: If using VPAT4 as a second V-sequence in the VSG active line, this value is the start position for second V-sequence.
31	[11:0]	0	V1TOG1_4	V1 Toggle Position 1
	[23:12]	0	V1TOG2_4	V1 Toggle Position 2
32	[11:0]	0	V1TOG3_4	V1 Toggle Position 3
	[23:12]	0	V2TOG1_4	V2 Toggle Position 1
33	[11:0]	0	V2TOG2_4	V2 Toggle Position 2
	[23:12]	0	V2TOG3_4	V2 Toggle Position 3
34	[11:0]	0	V3TOG1_4	V3 Toggle Position 1
	[23:12]	0	V3TOG2_4	V3 Toggle Position 2
35	[11:0]	0	V3TOG3_4	V3 Toggle Position 3
	[23:12]	0	V4TOG1_4	V4 Toggle Position 1
36	[11:0]	0	V4TOG2_4	V4 Toggle Position 2
	[23:12]	0	V4TOG3_4	V4 Toggle Position 3
37	[11:0]	0	V5TOG1_4	V5 Toggle Position 1
	[23:12]	0	V5TOG2_4	V5 Toggle Position 2
38	[11:0]	0	V5TOG3_4	V5 Toggle Position 3
	[23:12]	0	V6TOG1_4	V6 Toggle Position 1
39	[11:0]	0	V6TOG2_4	V6 Toggle Position 2
	[23:12]	0	V6TOG3_4	V6 Toggle Position 3
3A	[11:0]	0	FREEZE1_4	V1–V6 Freeze Position 1
	[23:12]	0	RESUME1_4	V1–V6 Resume Position 1
3B	[11:0]	0	FREEZE2_4	V1–V6 Freeze Position 2
	[23:12]	0	RESUME2_4	V1–V6 Resume Position 2

Table XXXI. V-Pattern Group 5 (VPAT5) Register Map

Address	Data Bit Content	Default Value	Register Name	Description
3C	[5:0] [11:6] [23:12]	0 0 0	VPOL_5 UNUSED VPATLEN_5	VPAT5 Start Polarity. V1[0].V2[1].V3[2].V4[3].V5[4].V6[5]. Unused. Total Length of VPAT5. Note: If using VPAT5 as a second V-sequence in the VSG active line, this value is the start position for second V-sequence.
3D	[11:0] [23:12]	0 0	V1TOG1_5 V1TOG2_5	V1 Toggle Position 1 V1 Toggle Position 2
3E	[11:0] [23:12]	0 0	V1TOG3_5 V2TOG1_5	V1 Toggle Position 3 V2 Toggle Position 1
3F	[11:0] [23:12]	0 0	V2TOG2_5 V2TOG3_5	V2 Toggle Position 2 V2 Toggle Position 3
40	[11:0] [23:12]	0 0	V3TOG1_5 V3TOG2_5	V3 Toggle Position 1 V3 Toggle Position 2
41	[11:0] [23:12]	0 0	V3TOG3_5 V4TOG1_5	V3 Toggle Position 3 V4 Toggle Position 1
42	[11:0] [23:12]	0 0	V4TOG2_5 V4TOG3_5	V4 Toggle Position 2 V4 Toggle Position 3
43	[11:0] [23:12]	0 0	V5TOG1_5 V5TOG2_5	V5 Toggle Position 1 V5 Toggle Position 2
44	[11:0] [23:12]	0 0	V5TOG3_5 V6TOG1_5	V5 Toggle Position 3 V6 Toggle Position 1
45	[11:0] [23:12]	0 0	V6TOG2_5 V6TOG3_5	V6 Toggle Position 2 V6 Toggle Position 3
46	[11:0] [23:12]	0 0	FREEZE1_5 RESUME1_5	V1–V6 Freeze Position 1 V1–V6 Resume Position 1
47	[11:0] [23:12]	0 0	FREEZE2_5 RESUME2_5	V1–V6 Freeze Position 2 V1–V6 Resume Position 2

Table XXXII. V-Pattern Group 6 (VPAT6) Register Map

Address	Data Bit Content	Default Value	Register Name	Description
48	[5:0] [11:6] [23:12]	0 0 0	VPOL_6 UNUSED VPATLEN_6	VPAT6 Start Polarity. V1[0].V2[1].V3[2].V4[3].V5[4].V6[5]. Unused. Total Length of VPAT6. Note: If using VPAT6 as a second V-sequence in the VSG active line, this value is the start position for second V-sequence.
49	[11:0] [23:12]	0 0	V1TOG1_6 V1TOG2_6	V1 Toggle Position 1 V1 Toggle Position 2
4A	[11:0] [23:12]	0 0	V1TOG3_6 V2TOG1_6	V1 Toggle Position 3 V2 Toggle Position 1
4B	[11:0] [23:12]	0 0	V2TOG2_6 V2TOG3_6	V2 Toggle Position 2 V2 Toggle Position 3
4C	[11:0] [23:12]	0 0	V3TOG1_6 V3TOG2_6	V3 Toggle Position 1 V3 Toggle Position 2
4D	[11:0] [23:12]	0 0	V3TOG3_6 V4TOG1_6	V3 Toggle Position 3 V4 Toggle Position 1
4E	[11:0] [23:12]	0 0	V4TOG2_6 V4TOG3_6	V4 Toggle Position 2 V4 Toggle Position 3
4F	[11:0] [23:12]	0 0	V5TOG1_6 V5TOG2_6	V5 Toggle Position 1 V5 Toggle Position 2

Table XXXII. V-Pattern Group 6 (VPAT6) Register Map (continued)

Address	Data Bit Content	Default Value	Register Name	Description
50	[11:0]	0	V5TOG3_6	V5 Toggle Position 3
	[23:12]	0	V6TOG1_6	V6 Toggle Position 1
51	[11:0]	0	V6TOG2_6	V6 Toggle Position 2
	[23:12]	0	V6TOG3_6	V6 Toggle Position 3
52	[11:0]	0	FREEZE1_6	V1–V6 Freeze Position 1
	[23:12]	0	RESUME1_6	V1–V6 Resume Position 1
53	[11:0]	0	FREEZE2_6	V1–V6 Freeze Position 2
	[23:12]	0	RESUME2_6	V1–V6 Resume Position 2

Table XXXIII. V-Pattern Group 7 (VPAT7) Register Map

Address	Data Bit Content	Default Value	Register Name	Description
54	[5:0]	0	VPOL_7	VPAT7 Start Polarity. V1[0]. V2[1]. V3[2]. V4[3]. V5[4]. V6[5].
	[11:6]	0	UNUSED	Unused.
	[23:12]	0	VPATLEN_7	Total Length of VPAT7. Note: If using VPAT7 as a second V-sequence in the VSG active line, this value is the start position for second V-sequence.
55	[11:0]	0	V1TOG1_7	V1 Toggle Position 1
	[23:12]	0	V1TOG2_7	V1 Toggle Position 2
56	[11:0]	0	V1TOG3_7	V1 Toggle Position 3
	[23:12]	0	V2TOG1_7	V2 Toggle Position 1
57	[11:0]	0	V2TOG2_7	V2 Toggle Position 2
	[23:12]	0	V2TOG3_7	V2 Toggle Position 3
58	[11:0]	0	V3TOG1_7	V3 Toggle Position 1
	[23:12]	0	V3TOG2_7	V3 Toggle Position 2
59	[11:0]	0	V3TOG3_7	V3Toggle Position 3
	[23:12]	0	V4TOG1_7	V4 Toggle Position 1
5A	[11:0]	0	V4TOG2_7	V4 Toggle Position 2
	[23:12]	0	V4TOG3_7	V4 Toggle Position 3
5B	[11:0]	0	V5TOG1_7	V5 Toggle Position 1
	[23:12]	0	V5TOG2_7	V5 Toggle Position 2
5C	[11:0]	0	V5TOG3_7	V5 Toggle Position 3
	[23:12]	0	V6TOG1_7	V6 Toggle Position 1
5D	[11:0]	0	V6TOG2_7	V6 Toggle Position 2
	[23:12]	0	V6TOG3_7	V6 Toggle Position 3
5E	[11:0]	0	FREEZE1_7	V1–V6 Freeze Position 1
	[23:12]	0	RESUME1_7	V1–V6 Resume Position 1
5F	[11:0]	0	FREEZE2_7	V1–V6 Freeze Position 2
	[23:12]	0	RESUME2_7	V1–V6 Resume Position 2

Table XXXIV. V-Pattern Group 8 (VPAT8) Register Map

Address	Data Bit Content	Default Value	Register Name	Description
60	[5:0]	0	VPOL_8	VPAT8 Start Polarity. V1[0]. V2[1]. V3[2]. V4[3]. V5[4]. V6[5].
	[11:6]	0	UNUSED	Unused.
	[23:12]	0	VPATLEN_8	Total Length of VPAT8. Note: If using VPAT8 as a second V-sequence in the VSG active line, this value is the start position for second V-sequence.
61	[11:0]	0	V1TOG1_8	V1 Toggle Position 1
	[23:12]	0	V1TOG2_8	V1 Toggle Position 2
62	[11:0]	0	V1TOG3_8	V1 Toggle Position 3
	[23:12]	0	V1TOG4_8	V1 Toggle Position 4

Table XXXIV. V-Pattern Group 8 (VPAT8) Register Map (continued)

Address	Data Bit Content	Default Value	Register Name	Description
63	[11:0] [23:12]	0 0	V2TOG1_8 V2TOG2_8	V2 Toggle Position 1 V2 Toggle Position 2
64	[11:0] [23:12]	0 0	V3TOG3_8 V3TOG4_8	V2 Toggle Position 3 V2 Toggle Position 4
65	[11:0] [23:12]	0 0	V3TOG1_8 V4TOG2_8	V3 Toggle Position 1 V3 Toggle Position 2
66	[11:0] [23:12]	0 0	V4TOG3_8 V4TOG4_8	V3 Toggle Position 3 V3 Toggle Position 4
67	[11:0] [23:12]	0 0	V5TOG1_8 V5TOG2_8	V4 Toggle Position 1 V4 Toggle Position 2
68	[11:0] [23:12]	0 0	V5TOG3_8 V6TOG4_8	V4 Toggle Position 3 V4 Toggle Position 4
69	[11:0] [23:12]	0 0	V6TOG1_8 V6TOG2_8	V5 Toggle Position 1 V5 Toggle Position 2
6A	[11:0] [23:12]	0 0	V6TOG3_8 V6TOG4_8	V5 Toggle Position 3 V5 Toggle Position 4
6B	[11:0] [23:12]	0 0	V6TOG1_8 V6TOG2_8	V6 Toggle Position 1 V6 Toggle Position 2
6C	[11:0] [23:12]	0 0	V6TOG3_8 V6TOG4_8	V6 Toggle Position 3 V6 Toggle Position 4
6D	[11:0] [23:12]	0 0	FREEZE1_8 RESUME1_8	V1–V6 Freeze Position 1 V1–V6 Resume Position 1
6E	[11:0] [23:12]	0 0	FREEZE2_8 RESUME2_8	V1–V6 Freeze Position 2 V1–V6 Resume Position 2
6F			UNUSED	Unused

Table XXXV. V-Pattern Group 9 (VPAT9) Register Map

Address	Data Bit Content	Default Value	Register Name	Description
70	[5:0] [11:6] [23:12]	0 0 0	VPOL_9 UNUSED VPATLEN_9	VPAT9 Start Polarity. V1[0]. V2[1]. V3[2]. V4[3]. V5[4]. V6[5]. Unused. Total Length of VPAT9. Note: If using VPAT9 as a second V-sequence in the VSG active line, this value is the start position for second V-sequence.
71	[11:0] [23:12]	0 0	V1TOG1_9 V1TOG2_9	V1 Toggle Position 1 V1 Toggle Position 2
72	[11:0] [23:12]	0 0	V1TOG3_9 V1TOG4_9	V1 Toggle Position 3 V1 Toggle Position 4
73	[11:0] [23:12]	0 0	V2TOG1_9 V2TOG2_9	V2 Toggle Position 1 V2 Toggle Position 2
74	[11:0] [23:12]	0 0	V3TOG3_9 V3TOG4_9	V2 Toggle Position 3 V2 Toggle Position 4
75	[11:0] [23:12]	0 0	V3TOG1_9 V4TOG2_9	V3 Toggle Position 1 V3 Toggle Position 2
76	[11:0] [23:12]	0 0	V4TOG3_9 V4TOG4_9	V3 Toggle Position 3 V3 Toggle Position 4
77	[11:0] [23:12]	0 0	V5TOG1_9 V5TOG2_9	V4 Toggle Position 1 V4 Toggle Position 2
78	[11:0] [23:12]	0 0	V5TOG3_9 V6TOG4_9	V4 Toggle Position 3 V4 Toggle Position 4

Table XXXV. V-Pattern Group 9 (VPAT9) Register Map (continued)

Address	Data Bit Content	Default Value	Register Name	Description
79	[11:0]	0	V6TOG1_9	V5 Toggle Position 1
	[23:12]	0	V6TOG2_9	V5 Toggle Position 2
7A	[11:0]	0	V6TOG3_9	V5 Toggle Position 3
	[23:12]	0	V6TOG4_9	V5 Toggle Position 4
7B	[11:0]	0	V6TOG1_9	V6 Toggle Position 1
	[23:12]	0	V6TOG2_9	V6 Toggle Position 2
7C	[11:0]	0	V6TOG3_9	V6 Toggle Position 3
	[23:12]	0	V6TOG4_9	V6 Toggle Position 4
7D	[11:0]	0	FREEZE1_9	V1–V6 Freeze Position 1
	[23:12]	0	RESUME1_9	V1–V6 Resume Position 1
7E	[11:0]	0	FREEZE2_9	V1–V6 Freeze Position 2
	[23:12]	0	RESUME2_9	V1–V6 Resume Position 2

Table XXXVI. Register Map Selection (SCK Updated Register)

Address	Data Bit Content	Default Value	Register Name	Register Description
7F	[0]	0	BANKSELECT2	Register Bank Access from Bank 2 to Bank 1. 0 = Bank 1, 1 = Bank 2.

Table XXXVII. V-Sequence 0 (VSEQ0) Register Map

Address	Data Bit Content	Default Value	Register Name	Description
80	[1:0]	0	HBLKMASK_0	Masking Polarity during HBLK. H1 [0]. H3 [1].
	[2]	0	CLPOBPOL_0	CLPOB Start Polarity
	[3]	0	PBLKPOL_0	PBLK Start Polarity
	[7:4]	0	VPATSEL_0	Selected V-Pattern Group for V-Sequence 0
	[9:8]	0	VMASK_0	Enable Masking of V-Outputs (Specified by Freeze/Resume Registers)
	[11:10]	0	HBLKALT_0	Enable HBLK Alternation
	[23:12]	0	UNUSED	Unused
81	[11:0]	0	VPATREPO_0	Number of Selected V-Pattern Group Repetitions for Odd Lines
	[23:12]	0	VPATREPE_0	Number of Selected V-Pattern Group Repetitions for Even Lines
82	[11:0]	0	VPATSTART_0	Start Position in the Line for the Selected V-Pattern Group
	[23:12]	0	HDLEN_0	HD Line Length (Number of Pixels) for V-Sequence 0
83	[11:0]	0	PBLKTOG1_0	PBLK Toggle Position 1 for V-Sequence 0
	[23:12]	0	PBLKTOG2_0	PBLK Toggle Position 2 for V-Sequence 0
84	[11:0]	0	HBLKTOG1_0	HBLK Toggle Position 1 for V-Sequence 0
	[23:12]	0	HBLKTOG2_0	HBLK Toggle Position 2 for V-Sequence 0
85	[11:0]	0	HBLKTOG3_0	HBLK Toggle Position 3 for V-Sequence 0
	[23:12]	0	HBLKTOG4_0	HBLK Toggle Position 4 for V-Sequence 0
86	[11:0]	0	HBLKTOG5_0	HBLK Toggle Position 5 for V-Sequence 0
	[23:12]	0	HBLKTOG6G	

Table XXXVIII. V-Sequence 1 (VSEQ1) Register Map

Address	Data Bit Content	Default Value	Register Name	Description
88	[1:0]	0	HBLKMASK_1	Masking Polarity during HBLK. H1 [0]. H3 [1].
	[2]	0	CLPOBPOL_1	CLPOB Start Polarity
	[3]	0	PBLKPOL_1	PBLK Start Polarity
	[7:4]	0	VPATSEL_1	Selected V-Pattern Group for V-Sequence 1
	[9:8]	0	VMASK_1	Enable Masking of V-) Outputs (Specified by Freeze/Resume Registers)
	[11:10]	0	HBLKALT_1	Enable HBLK Alternation
	[23:12]	0	UNUSED	Unused
89	[11:0]	0	VPATREPO_1	Number of Selected V-Pattern Group Repetitions for Odd Lines
	[23:12]	0	VPATREPE_1	Number of Selected V-Pattern Group Repetitions for Even Lines
8A	[11:0]	0	VPATSTART_1	Start Position in the Line for the Selected V-Pattern Group
	[23:12]	0	HDLEN_1	HD Line Length (Number of Pixels) for V-Sequence 1
8B	[11:0]	0	PBLKTOG1_1	PBLK Toggle Position 1 for V-Sequence 1
	[23:12]	0	PBLKTOG2_1	PBLK Toggle Position 2 for V-Sequence 1
8C	[11:0]	0	HBLKTOG1_1	HBLK Toggle Position 1 for V-Sequence 1
	[23:12]	0	HBLKTOG2_1	HBLK Toggle Position 2 for V-Sequence 1
8D	[11:0]	0	HBLKTOG3_1	HBLK Toggle Position 3 for V-Sequence 1
	[23:12]	0	HBLKTOG4_1	HBLK Toggle Position 4 for V-Sequence 1
8E	[11:0]	0	HBLKTOG5_1	HBLK Toggle Position 5 for V-Sequence 1
	[23:12]	0	HBLKTOG6_1	HBLK Toggle Position 6 for V-Sequence 1
8F	[11:0]	0	CLPOBTOG1_1	CLPOB Toggle Position 1 for V-Sequence 1
	[23:12]	0	CLPOBTOG2_1	CLPOB Toggle Position 2 for V-Sequence 1

Table XXXIX. V-Sequence 2 (VSEQ2) Register Map

Address	Data Bit Content	Default Value	Register Name	Description
90	[1:0]	0	HBLKMASK_2	Masking Polarity during HBLK. H1 [0]. H3 [1].
	[2]	0	CLPOBPOL_2	CLPOB Start Polarity
	[3]	0	PBLKPOL_2	PBLK Start Polarity
	[7:4]	0	VPATSEL_2	Selected V-Pattern Group for V-Sequence 2
	[9:8]	0	VMASK_2	Enable Masking of V-Outputs (Specified by Freeze/Resume Registers)
	[11:10]	0	HBLKALT_2	Enable HBLK Alternation
	[23:12]	0	UNUSED	Unused
91	[11:0]	0	VPATREPO_2	Number of Selected V-Pattern Group Repetitions for Odd Lines
	[23:12]	0	VPATREPE_2	Number of Selected V-Pattern Group Repetitions for Even Lines
92	[11:0]	0	VPATSTART_2	Start Position in the Line for the Selected V-Pattern Group
	[23:12]	0	HDLEN_2	HD Line Length (Number of Pixels) for V-Sequence 2
93	[11:0]	0	PBLKTOG1_2	PBLK Toggle Position 1 for V-Sequence 2
	[23:12]	0	PBLKTOG2_2	PBLK Toggle Position 2 for V-Sequence 2
94	[11:0]	0	HBLKTOG1_2	HBLK Toggle Position 1 for V-Sequence 2
	[23:12]	0	HBLKTOG2_2	HBLK Toggle Position 2 for V-Sequence 2
95	[11:0]	0	HBLKTOG3_2	HBLK Toggle Position 3 for V-Sequence 2
	[23:12]	0	HBLKTOG4_2	HBLK Toggle Position 4 for V-Sequence 2
96	[11:0]	0	HBLKTOG5_2	HBLK Toggle Position 5 for V-Sequence 2
	[23:12]	0	HBLKTOG6_2	HBLK Toggle Position 6 for V-Sequence 2
97	[11:0]	0	CLPOBTOG1_2	CLPOB Toggle Position 1 for V-Sequence 2
	[23:12]	0	CLPOBTOG2_2	CLPOB Toggle Position 2 for V-Sequence 2

Table XL. V-Sequence 3 (VSEQ3) Register Map

Address	Data Bit Content	Default Value	Register Name	Description
98	[1:0]	0	HBLKMASK_3	Masking Polarity during HBLK. H1 [0]. H3 [1].
	[2]	0	CLPOBPOL_3	CLPOB Start Polarity
	[3]	0	PBLKPOL_3	PBLK Start Polarity
	[7:4]	0	VPATSEL_3	Selected V-Pattern Group for V-Sequence 3
	[9:8]	0	VMASK_3	Enable Masking of V-Outputs (Specified by Freeze/Resume Registers)
	[11:10]	0	HBLKALT_3	Enable HBLK Alternation
	[23:12]	0	UNUSED	Unused
99	[11:0]	0	VPATREPO_3	Number of Selected V-Pattern Group Repetitions for Odd Lines
	[23:12]	0	VPATREPE_3	Number of Selected V-Pattern Group Repetitions for Even Lines
9A	[11:0]	0	VPATSTART_3	Start Position in the Line for the Selected V-Pattern Group
	[23:12]	0	HDLEN_3	HD Line Length (Number of Pixels) for V-Sequence 3
9B	[11:0]	0	PBLKTOG1_3	PBLK Toggle Position 1 for V-Sequence 3
	[23:12]	0	PBLKTOG2_3	PBLK Toggle Position 2 for V-Sequence 3
9C	[11:0]	0	HBLKTOG1_3	HBLK Toggle Position 1 for V-Sequence 3
	[23:12]	0	HBLKTOG2_3	HBLK Toggle Position 2 for V-Sequence 3
9D	[11:0]	0	HBLKTOG3_3	HBLK Toggle Position 3 for V-Sequence 3
	[23:12]	0	HBLKTOG4_3	HBLK Toggle Position 4 for V-Sequence 3
9E	[11:0]	0	HBLKTOG5_3	HBLK Toggle Position 5 for V-Sequence 3
	[23:12]	0	HBLKTOG6_3	HBLK Toggle Position 6 for V-Sequence 3
9F	[11:0]	0	CLPOBTOG1_3	CLPOB Toggle Position 1 for V-Sequence 3
	[23:12]	0	CLPOBTOG2_3	CLPOB Toggle Position 2 for V-Sequence 3

Table XLI. V-Sequence 4 (VSEQ4) Register Map

Address	Data Bit Content	Default Value	Register Name	Description
A0	[1:0]	0	HBLKMASK_4	Masking Polarity during HBLK. H1 [0]. H3 [1].
	[2]	0	CLPOBPOL_4	CLPOB Start Polarity
	[3]	0	PBLKPOL_4	PBLK Start Polarity
	[7:4]	0	VPATSEL_4	Selected V-Pattern Group for V-Sequence 4
	[9:8]	0	VMASK_4	Enable Masking of V-Outputs (Specified by Freeze/Resume Registers)
	[11:10]	0	HBLKALT_4	Enable HBLK Alternation
	[23:12]	0	UNUSED	Unused
A1	[11:0]	0	VPATREPO_4	Number of Selected V-Pattern Group Repetitions for Odd Lines
	[23:12]	0	VPATREPE_4	Number of Selected V-Pattern Group Repetitions for Even Lines
A2	[11:0]	0	VPATSTART_4	Start Position in the Line for the Selected V-Pattern Group
	[23:12]	0	HDLEN_4	HD Line Length (Number of Pixels) for V-Sequence 4
A3	[11:0]	0	PBLKTOG1_4	PBLK Toggle Position 1 for V-Sequence 4
	[23:12]	0	PBLKTOG2_4	PBLK Toggle Position 2 for V-Sequence 4
A4	[11:0]	0	HBLKTOG1_4	HBLK Toggle Position 1 for V-Sequence 4
	[23:12]	0	HBLKTOG2_4	HBLK Toggle Position 2 for V-Sequence 4
A5	[11:0]	0	HBLKTOG3_4	HBLK Toggle Position 3 for V-Sequence 4
	[23:12]	0	HBLKTOG4_4	HBLK Toggle Position 4 for V-Sequence 4
A6	[11:0]	0	HBLKTOG5_4	HBLK Toggle Position 5 for V-Sequence 4
	[23:12]	0	HBLKTOG6_4	HBLK Toggle Position 6 for V-Sequence 4
A7	[11:0]	0	CLPOBTOG1_4	CLPOB Toggle Position 1 for V-Sequence 4
	[23:12]	0	CLPOBTOG2_4	CLPOB Toggle Position 2 for V-Sequence 4